Simulink® Design Verifier™ Release Notes

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Simulink® Design Verifier™ Release Notes

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Summary by Version

This table provides quick access to what's new in each version. For clarification, see "Using Release Notes" on page 1.

Version (Release)	New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Latest Version V1.5 (R2009b)	Yes Details	Yes Summary	Bug Reports Includes fixes	Printable Release Notes: PDF Current product documentation
V1.4 (R2009a)	Yes Details	No	Bug Reports Includes fixes	Printable Release Notes: PDF Current product documentation
V1.3 (R2008b)	Yes Details	Yes Summary	Bug Reports Includes fixes	Printable Release Notes: PDF Current product documentation
V1.2.1 (R2008a+)	No	No	Bug Reports Includes fixes	No
V1.2 (R2008a)	Yes Details	No	Bug Reports Includes fixes	No
V1.1.1 (R2007b+)	No	No	Bug Reports Includes fixes	No
V1.1 (R2007b)	Yes Details	No	Bug Reports Includes fixes	No
V1.0 (R2007a+)	Yes Details	No	Bug Reports	No

Using Release Notes

Use release notes when upgrading to a newer version to learn about:

- New features

- Changes

- Potential impact on your existing files and practices

Review the release notes for other MathWorks™ products required for this product (for example, MATLAB® or Simulink®). Determine if enhancements, bugs, or compatibility considerations in other products impact you.

If you are upgrading from a software version other than the most recent one, review the current release notes and all interim versions. For example, when you upgrade from V1.0 to V1.2, review the release notes for V1.1 and V1.2.

What Is in the Release Notes

New Features and Changes

- New functionality

- Changes to existing functionality

Version Compatibility Considerations

When a new feature or change introduces a reported incompatibility between versions, the **Compatibility Considerations** subsection explains the impact.

Compatibility issues reported after the product release appear under Bug Reports at The MathWorks™ Web site. Bug fixes can sometimes result in incompatibilities, so review the fixed bugs in Bug Reports for any compatibility impact.

Fixed Bugs and Known Problems

The MathWorks offers a user-searchable Bug Reports database so you can view Bug Reports. The development team updates this database at release time and as more information becomes available. Bug Reports include provisions for any known workarounds or file replacements. Information is available for bugs existing in or fixed in Release 14SP2 or later. Information is not available for all bugs in earlier releases.

Access Bug Reports using your MathWorks Account.

Version 1.5 (R2009b) Simulink Design Verifier Software

This table summarizes what's new in V1.5 (R2009b):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	Yes Summary	Bug Reports	Printable Release Notes: PDF Current product documentation

- "New Functions for Verification Objectives and Constraints" on page 4
- "Support for Enumerated Signals and Parameters" on page 5
- "New Option to Stop Simulation on Proof Violation" on page 5
- "New sldvmakeharness Function" on page 6
- "New sldvreport Function" on page 6
- "New Support for Simulink Blocks" on page 6
- "Support for New Blocks" on page 6

New Functions for Verification Objectives and Constraints

Use these four new functions to specify objectives and constraints within an Embedded MATLAB™ script. You can use these functions instead of the corresponding Simulink® Design Verifier™ blocks.

Function	Purpose	Corresponding Block
sldv.assume	Proof assumption	Proof Assumption
sldv.condition	Test condition	Test Condition
sldv.prove	Proof objective	Proof Objective
sldv.test	Test objective	Test Objective

These functions:

- Identify mathematical relationships for objectives and constraints in a form that can be more natural than using block parameters
- Support specifying multiple constraints without complicating the model
- Provide access to the power of the MATLAB software
- Support separation of verification and model design

Compatibility Considerations
The following functions will be removed in a future release:

- `dv.assume`
- `dv.condition`
- `dv.prove`
- `dv.test`

To ensure models with those functions will work in future releases, replace these functions with the corresponding new function added in this release. For example, replace `dv.assume` with `sldv.assume`.

Support for Enumerated Signals and Parameters
The Simulink Design Verifier software now supports Simulink models with enumerations. All the Simulink Design Verifier library blocks support enumerated parameters, constants, and inputs.

New Option to Stop Simulation on Proof Violation
The Simulink Design Verifier software allows you to stop a model simulation if it encounters a property violation. You enable this capability by inserting a Proof Objective block into a model and setting the **Stop simulation when the property is violated** parameter. If the simulation detects a violation of the property specified in the Proof Objective block, it terminates with an error.

Therefore, you can now verify a counterexample that was detected during a Simulink Design Verifier analysis.

New sldvmakeharness Function

With the new `sldvmakeharness` function, you can:

- Create a test harness model from existing Simulink Design Verifier analysis data.

- Create an empty test harness model directly from a Simulink model.

New sldvreport Function

You can now generate and customize a report from existing Simulink Design Verifier analysis data with the new `sldvreport` function.

New Support for Simulink Blocks

The Simulink Design Verifier software now supports the following blocks and parameters:

- Direct Lookup Table (n-D)

- Discrete Transfer Fcn

- Lookup Table and Lookup Table (2-D) — Unless the **Lookup method** block parameter specifies `Interpolation-Extrapolation` and the block's input and output signals do not have the same floating-point data type.

- Math Function — All signal types now support the `hermitian` and `transpose` function parameter settings

- Rate Limiter — For signals of all data types

- Shift Arithmetic — For all parameters and signals of all data types

- Tapped Delay

- Transfer Fcn Direct Form II

- Transfer Fcn Direct Form II Time Varying

Support for New Blocks

The Simulink Design Verifier software supports the following new Simulink blocks:

- Discrete PID Controller

- Discrete PID Controller (2 DOF)

- Enumerated Constant

Version 1.4 (R2009a) Simulink Design Verifier Software

This table summarizes what's new in V1.4 (R2009a):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	Printable Release Notes: PDF Current product documentation

New features and changes introduced in this version are:

- "Automatic Stubbing for Unsupported Operations" on page 8
- "Long Test Case Optimization" on page 9
- "New Support for Blocks" on page 9
- "Analyzing External M-Files for Embedded MATLAB Function Blocks" on page 9
- "Enhanced Block Replacement Capability for Subsystems and Model Blocks" on page 10
- "New Implies Block" on page 10
- "New Property-Proving Examples and Demos" on page 10
- "sldvisactive Function" on page 11

Automatic Stubbing for Unsupported Operations

Automatic stubbing allows you to complete a test-generation or property-proving analysis even if the model contains blocks or functions that the Simulink Design Verifier software does not support, like S-functions and C math operations.

By default, this feature is unavailable. To enable automatic stubbing before running an analysis, on the Configuration Parameters **Design Verifier** main pane, select **Automatic stubbing of unsupported blocks and functions**.

In addition, if the compatibility check finds unsupported blocks that automatic stubbing can handle, you can enable automatic stubbing at that time.

Long Test Case Optimization

`Long test cases` is a new option for the **Test suite optimization** parameter. The `Long test cases` option instructs the Simulink Design Verifier software to create fewer but longer test cases that each satisfy multiple test objectives. With this option, you can customize the analysis results, run a more efficient analysis, and create easier-to-review results, in both Signal Builder and in the HTML report that the software generates.

New Support for Blocks

The Simulink Design Verifier software now supports models containing the following blocks:

- Combinatorial Logic
- Decrement Time To Zero
- Discrete Filter
- Fixed-Point State-Space
- Integer Delay
- Model blocks that reference other models
- Prelookup
- Relay

Analyzing External M-Files for Embedded MATLAB Function Blocks

If your model contains an Embedded MATLAB Function block that calls any external M-files, the Simulink Design Verifier software can now accumulate coverage results for those M-files.

Enhanced Block Replacement Capability for Subsystems and Model Blocks

You can write your own replacement rules to replace subsystem or Model blocks that reference another model with theSimulink Design Verifier block replacement capability. The software replaces a subsystem or Model block with a different subsystem or with a built-in block as defined in the block replacement rules.

New Implies Block

The new Implies block simplifies property specification. You can now specify conditions that produce a given response. For example, you can quickly create expressions indicating that pressing the break pedal implies the cruise control must be inactive.

You can use the Implies block in any model, not just when running the Simulink Design Verifier software.

New Property-Proving Examples and Demos

The Simulink Design Verifier block library includes four new example models that demonstrate how to define complex properties for property-proving analysis.

In addition, the following demo models are shipping with R2009a:

- `sldvdemo_sbr_design.mdl` — Finding property violations

- `sldvdemo_sbr_verification.mdl` — Proving that properties are valid

- `sldvdemo_thrustrvs_verification.mdl` — Analyzing model and properties to prove correctness or to identify counterexamples

- `sldvdemo_cruise_control_fxp_verification.mdl` — Proving properties for fixed-point arithmetic with block replacements

- `sldvdemo_cruise_control_verification.mdl` — Supporting model reference and verification subsystems

sldvisactive Function

The `sldvisactive` function checks whether the Simulink Design Verifier software is actively translating the model. This function is called from the masked initialization of masked subsystems and other model or block callbacks to configure the model, as needed, for Simulink Design Verifier analysis.

For example, the mask initialization of the Environment Controller block invokes the `sldvisactive` function to output the signal at its Sim port when you start analyzing a model that contains the block.

Version 1.3 (R2008b) Simulink Design Verifier Software

This table summarizes what's new in V1.3 (R2008b):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	Yes Summary	Bug Reports	Printable Release Notes: PDF Current product documentation

New features and changes introduced in this version are:

- "Simulink Bus Signals and Bus Objects Support " on page 12
- "Fixed-Point Data Support" on page 13
- "Generating Test Harness Model with Model Reference" on page 13
- "Generating SystemTest TEST-File" on page 13
- "Improved Search Algorithms" on page 13
- "New Data File Format" on page 14
- "New HTML Report" on page 14
- "Blocks with No Input Ports Limitation" on page 15

Simulink Bus Signals and Bus Objects Support

Simulink Design Verifier now supports Simulink buses and bus objects:

- The root Inport and Outport blocks accept bus signals.
- Nonvirtual buses are propagated through the model elements.
- The test harness model reconstructs the needed bus signals from the underlying bus elements.

Fixed-Point Data Support

Simulink Design Verifier blocks now support fixed-point parameters and inputs. These blocks include:

- Test Condition

- Test Objective

- Assumption

- Proof Objective

The `Slvd.Point` and `Sldv.Interval` constructors now accept fixed-point data.

Generating Test Harness Model with Model Reference

To use this option, select **Reference input model in generated harness** in the **Design Verifier > Results** pane of the Configuration Parameters dialog box. Simulink Design Verifier software then uses model reference to run the original model from the test harness.

Generating SystemTest TEST-File

To use this option, select **Save test harness as SystemTest TEST-File** in the **Design Verifier > Results** pane of the Configuration Parameters dialog box. The software creates a TEST-file instead of a test harness model. Using a TEST-file allows you to run the test cases in the SystemTest™ environment and configure the model coverage settings using the SystemTest software.

Improved Search Algorithms

This release includes search algorithms for the following two modes that improve the performance and the quality of the results:

- Test case generation — The combined objectives options minimizes the number of test cases by generating cases that address more than one test objective.

- Property proving — Proving that model properties are valid.

New Data File Format

When the Simulink Design Verifier software completes an analysis, it creates a data file. Now the data file supports bus input ports and includes more information about the analyzed model. For more information, see "Examining Simulink Design Verifier Data Files" in the Simulink Design Verifier documentation.

Compatibility Considerations

To convert an sldvData structure from the old format to the new format, use the Sldv.DataUtils.convertToCurrentFormat utility with the following syntax:

```
new_sldvData = Sldv.DataUtils.convertToCurrentFormat(model, old_sldvData)
```

The arguments used for this conversion comprise:

- model — The name of the model that was analyzed

- old_sldvData — The name of an sldvData structure created using the old (pre-R2008b) format

To convert an sldvData structure in the new format to the old format, use the Sldv.DataUtils.convertToOldFormat utility with the following syntax:

```
old_sldvData = Sldv.DataUtils.convertToOldFormat(model, new_sldvData)
```

The arguments used for this conversion comprise:

- model — The name of the model that was analyzed

- new_sldvData — The name of an sldvData structure created using the format that is new with R2008b

New HTML Report

The HTML report that Simulink Design Verifier software generates has been enhanced. Now, when you select **Generate report of the results** in the **Design Verifier > Report** pane of the Configuration Parameters dialog box, the report generated has several improvements:

- The report generates faster and is easier to understand.

- The report can display expected outputs.

- The software generates a report that reflect the analysis settings (for example, test case generation vs. property proving).

Blocks with No Input Ports Limitation

If a Simulink model has any blocks with no input ports, Simulink Design Verifier software cannot generate the test harness.

Version 1.2 (R2008a) Simulink Design Verifier Software

This table summarizes what's new in V1.2 (R2008a):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	Printable Release Notes: PDF Current product documentation

New features and changes introduced in this version are

- "Embedded MATLAB Subset Support" on page 16
- "Enhanced Support for Stateflow Truth Tables" on page 16
- "New Simulink® Design Verifier Data File Options" on page 16
- "New Test Suite Optimization Setting" on page 17

Embedded MATLAB Subset Support

This release provides support for the Embedded MATLAB Function block in the Simulink software and Embedded MATLAB functions in the Stateflow® software. For more information, see "Support Limitations for the Embedded MATLAB Subset" in the *Simulink Design Verifier User's Guide*.

Enhanced Support for Stateflow Truth Tables

Previous releases support only the Stateflow Classic truth tables. However, this release introduces support for Embedded MATLAB truth tables in the Stateflow software, which includes support for the Truth Table block. See "Truth Table Functions" in the Stateflow documentation for more information.

New Simulink Design Verifier Data File Options

This release introduces new options on the **Design Verifier > Results** pane of the Configuration Parameters dialog box:

- **Include expected output values** — Simulates the model using the test case signals and includes the output values in the Simulink Design Verifier data file. See "Include expected output values" for more information.

- **Randomize data that does not affect outcome** — Assigns random values instead of zeros to input signals that have no impact on test or proof objectives. See "Randomize data that does not affect outcome" for more information.

New Test Suite Optimization Setting

In this release, the **Test suite optimization** parameter that appears on the **Design Verifier > Test Generation** pane of the Configuration Parameters dialog box includes a new setting: Large model. This test generation strategy is tailored to large, complex models that contain nonlinearities and many test objectives. See "Test suite optimization" for more information.

Version 1.1 (R2007b) Simulink Design Verifier Software

This table summarizes what's new in V1.1 (R2007b):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	No

Fixed-Point Data Type Support

This release provides support for fixed-point data types. For more information, see "Fixed-Point Support Limitations" in the *Simulink Design Verifier User's Guide*.

Version 1.0 (R2007a+) Simulink Design Verifier Software

This table summarizes what's new in V1.0 (R2007a+):

New Features and Changes	Version Compatibility Considerations	Fixed Bugs and Known Problems	Related Documentation at Web Site
Yes Details below	No	Bug Reports	No

Version 1.0 of the Simulink Design Verifier software was released in a Web-downloadable form after R2007a.

Introducing the Simulink Design Verifier Software

The Simulink Design Verifier software extends the Simulink and Stateflow products with formal methods that help you confirm your models and charts behave correctly. The Simulink Design Verifier software performs a mathematically rigorous analysis of your model to identify all of its possible execution pathways. Subsequently, the software can

- **Generate Tests**

  The Simulink Design Verifier software can generate tests that satisfy your model's coverage objectives, including decision coverage, condition coverage, and modified condition/decision coverage (MC/DC). You can even customize the tests that it generates by using Simulink Design Verifier blocks that allow you to specify your own objectives and to constrain signal values. After the software completes its analysis, it produces a test harness model with a Signal Builder block that contains test signals. Simply simulate the test harness model to confirm that the test signals achieve your model's objectives.

- **Prove Properties**

  The Simulink Design Verifier software can prove that signals in your model attain particular values or ranges. Use Simulink Design Verifier blocks to specify values and ranges that you desire signals to attain, or to constrain the values of other signals. If the software disproves any of the values or ranges given the constraints you specify, it produces a test

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harness model with a Signal Builder block that contains signals comprising counterexamples. Simply simulate the test harness model to confirm that the counterexamples falsify your model's properties.

The Simulink Design Verifier software documents its analysis results in an HTML report. Also, it produces a data file containing the analysis results, which you can postprocess for your own analyses and reports.

In short, the Simulink Design Verifier software gives you confidence in the behavior of your Simulink models and Stateflow charts.

Compatibility Summary for Simulink Design Verifier Software

This table summarizes new features and changes that might cause incompatibilities when you upgrade from an earlier version, or when you use files on multiple versions. Details are provided in the description of the new feature or change.

Version (Release)	New Features and Changes with Version Compatibility Impact
Latest Version **V1.5 (R2009b)**	See the **Compatibility Considerations** subheading for: • "New Functions for Verification Objectives and Constraints" on page 4
V1.4 (R2009a)	None
V1.3 (R2008b)	See the **Compatibility Considerations** subheading for: • "New Data File Format" on page 14
V1.2 (R2008a)	None
V1.1 (R2007b)	None
V1.0 (R2007a+)	None